IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicants:	Lane et al.		
U.S. Appl. No.:	10/830,188	Group:	2822
Filed:	April 21, 2004	Examiner:	PERKINS, Pamela E.
For:	METHOD FOR ACCOMMODATING SMALL MINIMUM DIE IN WIRE BONDED AREA ARRAY PACKAGES		

BRIEF ON APPEAL UNDER 37 C.F.R. § 41.37

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 223 13-1450

Sir:

Further to the Office Action dated November 3, 2005 and Notice of Appeal filed on May 3, 2007, this Appeal Brief is respectfully submitted. The fees required under § 41.37(a) should be charged to Deposit Account 17-0026.

This brief contains items under the following headings as required by C.F.R. § 41.37 and M.P.E.P. § 1206:

I. Real Party in Interest
II. Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Claimed Subject Matter
VI. Grounds of Rejection to be Reviewed on Appeal
VII. Argument
VIII. Claims
IX. Evidence
X. Related Proceedings

Appendix A. Claims
Appendix B: Evidence
Appendix C: Related Proceedings

I. Real Party in Interest

The real party in interest for this Application is Qualcomm Incorporated as evidenced by the assignment documents recorded at Reel: 014753, Frame: 0344.

II. Related Appeals and Interferences

To the best of Appellants' knowledge, there are no other prior or pending appeals of this Application, or patent interference proceedings, or judicial proceedings which may be related to, directly affect, or be directly affected by, or have a bearing on the Board's decision of this Appeal.

III. Status of Claims

In the Application on appeal, claims 1-12 and 14 are pending. Claims 1 and 12 are independent. Claims 1-12 and 14 are finally rejected and are on appeal. Claims 13 and 15 were canceled.

IV. Status of Amendments

The Amendment filed on May 4, 2005, has been entered (as stated on page 2 of the Final Office Action mailed on November 3, 2005).

V. Summary of the Claimed Subject Matter

Independent claim 1 is directed to a method for making a high pin-count die (201, 801) by providing a substrate (205, 805) and forming a die attach area onto the substrate for mounting a die. The die (201, 801) has at least one bond pad (202, 802). At least one bond island (206, 806) is located on the substrate (205, 805). The

bond pad (202, 802) is connected to the bond island (206, 806) with a wire bond (204, 804), and a plurality of solder balls (810) are connected to the at least one bond island (206, 806). The plurality of solder balls (810) are located inwardly from an edge of the substrate (205, 805). At least one redundant solder ball (609) in Fig. 6 is used to form a path for the inner solder balls connected to bond islands (206, 806) which are to be electrically plated.

Independent claim 12 is directed to a method for providing an area array package (200, 800) by providing a substrate (205, 805) and attaching one or more die (201, 801) to the substrate. The die (801) is wire bonded to the substrate (205, 805), and the wires (204, 804) and die are encapsulated on the substrate by an enclosure (820). A plurality of solder balls (810) are coupled to the at least one of a plurality of bond islands (206, 806) located on the substrate (805). At least one redundant solder ball (609) in Fig. 6 is used to form a path for the inner solder balls connected to bond islands (206, 806) which are to be electrically plated.

VI. Grounds of Rejection to be Reviewed on Appeal

In the Office Action dated November 3, 2005, claims 1-5, 11 and 12 are finally rejected under 35 USC 103(a) as being unpatentable over Torres et al. (U.S. Patent 5,898,213, hereinafter referred to as "Torres") in view of Lin et al. (U.S. Patent 5,468,999, hereinafter referred to as "Lin"). Claims 6-10 and 14 are finally rejected under 35 USC 103(a) as being unpatentable over Torres in view of Lin as applied to claim 1 and further in view of Chou et al. (U.S. Patent 5,691,568, hereinafter referred to as "Chou"). This final rejection was appealed on May 3, 2006.

VII. Argument

In rejecting claims under 35 U.S.C. §103, it is incumbent on the Examiner to establish a factual basis to support the legal conclusion of obviousness. See, In re Fine, 837 F.2d 1071, 1073; 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17; 148 USPQ 459, 467 (1966), and to provide a reason why one of ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention.

Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal Inc. v. F-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933. The Examiner may not pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve Inc., 796 F.2d 443, 448, 230 USPQ 416, 419 (Fed. Cir. 1986), cert. denied, 484 U.S. 823 (1987) and In re Kamm, 452 F.2d 1052, 1057, 172 USPQ 298, 301-2 (CCPA 1972), and obviousness cannot be established by locating references which describe various aspects of Appellants' invention without also providing evidence of the motivating force which would impel one skilled in the art to

do what Appellants have done. Ex parte Levengood, 28 USPQ2d 1300, 1302 (Bd. App. & Int. 1993). These showings by the Examiner are an essential part of complying with the burden of presenting a *prima facie* case of obviousness. These showings must be clear and particular, and broad conclusory statements about the teaching of multiple references, standing alone, are not "evidence." See In re Dembiczak, 175 F.3d 994 at 1000, 50 USPQ2d 1614 at 1617 (Fed. Cir. 1999). Note, In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992). To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be suggested or taught by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1970). All words in a claim must be considered in judging the patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). Moreover, a factual inquiry whether to modify a reference must be based on objective evidence of record, not merely conclusory statements of the Examiner. See, In re Lee, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).

Independent claims 1 and 12 are directed to methods for making a high pin-count die or an area array package by providing a substrate and forming a die attach area onto the substrate for mounting a die. The die has at least one bond pad, and at least one bond island that is located onto the substrate. The bond pad is connected to the bond island with a wire bond, and a plurality of solder balls are connected to the at least one bond island. The plurality of solder balls is located

inwardly from an edge of the substrate. At least one redundant solder ball is used to form a path for the inner solder balls connected to bond islands which are to be electrically plated.

It is respectfully submitted that the Torres patent neither discloses the claimed connecting of the solder balls nor using at least one redundant solder ball to form a path for the inner solder balls connected to bond islands which are to be electrically plated. The Office Action acknowledges the shortcomings of Torres, and it states on the bottom of page 2, that "Torres et al. do not disclose connecting a plurality of solder balls to at least one bond island, wherein at least one redundant solder ball is used to form a path for the inner solder balls connected to bond islands to be electrically plated." The Office Action, however, further alleges on page 3 that Lin recites such a feature at col. 4, lines 55-64. The Appellants respectfully disagree.

Appellants respectfully submit that Lin does not teach, show or suggest the limitations missing from Torres, and more specifically Lin does not disclose the claimed connecting of the solder balls and using at least one redundant solder ball to form a path for the inner solder balls connected to bond islands to be electrically plated. The portion of Lin identified and relied upon in the Office Action states:

> Although not apparent in FIG. 2, conductive vias 22 are typically openings in the substrate having plated sidewalls (as opposed to being filled vias). On the bottom of each of the substrates the conductive vias 22 are further routed by a plurality of conductive traces 30 (not all shown) which terminate into conductive terminal pads 32. Attached to each conductive terminal pad 32 is a conductive ball 34 such as conductive solder balls or conductor coated polymer spheres. In accordance with the present invention, a configuration of conductive terminal pads and conductive balls on the bottom of the package substrate is in an array configuration as opposed to being in a purely peripheral configuration.

Appellants respectfully submit that the only reference to solder balls in Lin is in the quoted passage above. Appellants further submit that Lin does not recite

or even suggest the claimed use of at least one redundant solder ball to form a path for the inner solder balls connected to bond islands to be electrically plated.

In order to more clearly appreciate what Lin actually discloses, Figure 3 of Lin is reproduced below:

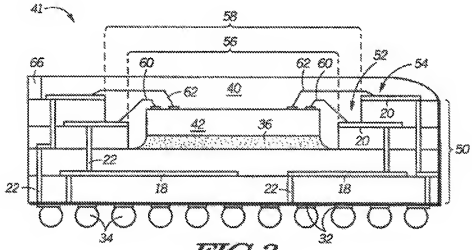

FIG.3

At most, Lin discloses a ball grid semiconductor array having a solder ball 34 for each of the conductive terminal pads 32. Accordingly, the Office Action fails to set forth a *prima facie* case of unpatentability under 35 USC 103(a), because the cited references do not disclose all the claimed limitations of independent claims 1 and 12 relating to the at least one redundant solder ball which is used to form a path for the inner solder balls connected to bond islands to be electrically plated.

If the cited Torres and Lin references are combined as suggested in the Office Action, the skilled artisan would merely replace the solder balls (described but not illustrated) of Torres with the solder balls 34 and the terminal pads 32 of Lin. There is no motivation to make such a substitution, because Torres discloses both solder

balls and conductive terminal pads. (See col. 5, lines 30-31). Assuming for the purposes of argument that the skilled artisan would combine Torres and Lin, the resulting hypothetical system of Torres in view of Lin would simply provide a ball grid array with Lin's solder balls and a corresponding terminal pad. The resulting hypothetical system, however, would **not** provide a ball grid array with the at least one redundant solder ball which is used to form a path for the inner solder balls connected to bond islands which are to be electrically plated, as claimed by Appellants. Since the resulting hypothetical combination of Torres and Lin is missing essential claim limitations of independent claims 1 and 12, the rejection under 35 USC 103(a) is improper and must be withdrawn.

The Dependent Claims

Since dependent claims 2-11 and 14 depend from allowable independent claims 1 and 12, it is respectfully submitted that the dependent claims should be patentable over the cited prior art for at least the same reasons as independent claims 1 and 12.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Appellants on May 4, 2005.

IX. EVIDENCE

No evidence pursuant to 37 CFR §§ 1.130, 1.131, or 1.132 or entered by or

relied upon by the Examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in Section II, above.

CONCLUSION

Appellants respectfully submit that the pending claims are patentable over the applied art and that all of the rejections and objections of record should be reversed.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 17-0026 for any additional fees required under 37 C.F.R. § 1.16 or 1.17, particularly extension of time fees.

Dated: April 30, 2007

Respectfully submitted,

By _____

William Marcus Hooks
Registration No.: 48,857
QUALCOMM Incorporated
5775 Morehouse Drive
San Diego, CA 92121-1714
(858) 658-5932
Attorney for Appellants

APPENDIX A: CLAIMS

Listing of Claims:

1. **(previously presented)** A method for making a high pin-count die, comprising the steps of:

providing a substrate;

forming a die attach area onto the substrate for mounting a die, the die having at least one bond pad;

locating at least one bond island onto the substrate;

connecting the bond pad to the bond island with a wire bond; and

connecting a plurality of solder balls to the at least one bond island, the plurality of solder balls being located inwardly from an edge of the substrate,

wherein at least one redundant solder ball is used to form a path for the inner solder balls connected to bond islands to be electrically plated.

2. **(original)** The method of claim 1, further comprising the step of encapsulating the die.

3. **(original)** The method of claim 1, further comprising forming a trace between the bond island and a package lead located on the substrate.

4. **(original)** The method of claim 3, wherein the package lead is a solder ball included in a ball grid array (BGA).

5. **(original)** The method of claim 3, wherein the package lead is a land included in a land grid array (LGA).

6. **(original)** The method of claim 1, further comprising the step of depositing a bond finger onto the substrate.

7. **(original)** The method of claim 6, further comprising the step of bonding a wire between the bond finger and the bond pad.

8. **(original)** The method of claim 6, further comprising the step of forming a trace between the bond finger and a package lead.

9. **(original)** The method of claim 8, wherein the package lead is a solder ball included in a ball grid array (BGA).

10. **(original)** The method of claim 8, wherein the package lead is a land in a land grid array (LGA).

11. **(original)** The method of claim 1, further comprising the step of forming a plurality of die attach areas on the substrate for mounting a plurality of die.

12. **(previously presented)** A method for providing an area array package, comprising the steps of:

providing a substrate;

attaching one or more die to the substrate;

wire bonding the die to the substrate;

encapsulating the wires and die on the substrate; and

coupling a plurality of solder balls to the at least one of a plurality of bond islands located on the substrate,

wherein at least one redundant solder ball is used to form a path for the inner solder balls connected to bond islands to be electrically plated.

13. **(canceled)**

14. **(previously presented)** The method of claim 12, further comprising the step of coupling a plurality of bond fingers located on the substrate to the solder balls or the bond islands.

15. **(canceled)**

APPENDIX B: EVIDENCE

(None)

APPENDIX C: RELATED PROCEEDINGS

(None)